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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: WOLFRAM KLUGE DIETMAR EGGERT	Examiner: B. Jackson
Serial No.: 09/904,951	Group Art Unit: 2685
Filed: July 13, 2001	Att'y Docket: 2000.066200
For: MIXER	Customer No. 023720

APPEAL BRIEF

CERTIFICATE OF MAILING
37 C.F.R. 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:

05.04.05 (Date) Kathy Dorsey (Signature)

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences in response to the final Office Action mailed on October 21, 2004. A Notice of Appeal was filed March 17, 2005, so this Appeal Brief is believed to be timely filed.

The Assistant Commissioner is authorized to deduct the fee for filing this Appeal Brief ($500) from **Advanced Micro Devices, Inc.'s Deposit Account 01-0365/DE0029.** Should funds be insufficient, the Commissioner is authorized to deduct any and all required fees from Williams, Morgan & Amerson's P.C. Deposit Account 50-0786/2000.066200.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc. The assignment of the present application to Advanced Micro Devices, Inc., is recorded at Reel 12464, Frame 0405.

II. RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-18 are pending in the present application. Claims 1-3 and 12-14 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Durec (U.S. Patent No. 6,144,846) in view of Razavi, et al (U.S. Patent No. 6,748,204). Claims 4-11 and 15-18 stand rejected as allegedly being obvious over Bojer, et al (U.S. Patent No. 6,029,059) in view of Ravazi and Durec.

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 sets forth a mixer, which includes a multiplier circuit having a first and a second mixer. The first mixer includes a first number of transistors and the second mixer includes a second number of transistors. The first number is different than the second number. The mixer also includes a generator for generating two first and two second control signals for

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controlling said first and second mixers. The two first control signals have a frequency f_1 and the two second control signals have a different frequency f_2.

One exemplary embodiment of a mixer such as set forth in claim 1 is shown in Figure 1. The exemplary embodiment of the mixer includes a first mixer having two transistors 13, 16 and a second mixer having four transistors 11, 12, 14, 15. The mixer shown in Figure 1 also includes a generator, which includes a voltage controlled oscillator (VCO) 20 and a frequency derivation circuit 30, for generating two first and two second control signals 21, 22, 23, 24, respectively, for controlling said first and second mixers. The two first control signals have a frequency f_1 and the two second control signals have a different frequency f_2. See Patent Application, page 9, ll. 14-19.

Independent claim 4 sets forth a mixer for I/Q quadrature signal generation. The mixer set forth in claim 4 includes a first multiplier circuit having a first and a second mixer. The first mixer includes a first number of transistors and the second mixer includes a second number of transistors. The first number is different than the second number. The mixer also includes a second multiplier circuit having a third and a fourth mixer. The third mixer includes a third number of transistors and the fourth mixer includes a fourth number of transistors. The third number is different than the fourth number. The mixer also includes a generator for generating two first and two second control signals for controlling said first and second mixers and two third and two fourth control signals for controlling said third and fourth mixers. The two first, two second, two third, and two fourth control signals are in each case balanced signals. The two first and two third control signals have a frequency f_1 and the two second and two fourth control signals have a different frequency f_2. Either said signals at frequency f_1 or at frequency f_2 are provided in four phases each shifted by $\pi/2$.

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One exemplary embodiment of a mixer such as set forth in claim 4 is shown in Figure 3. The exemplary embodiment of the mixer includes first and second multiplier circuits, *e.g.*, the Gilbert cell circuits 10, 40, which include first, second, third, and fourth numbers of transistors. The mixer also includes a frequency derivation circuit 30 for generating two first and two second control signals 21, 22, 23, 24 for controlling said first and second mixers and two third and two fourth control signals 25, 26, 27, 28 for controlling said third and fourth mixers. See Patent Application, page 12, line 19 – page 13, line 10.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant respectfully requests that the Board review and overturn the two rejections present in this case. The following issues are presented on appeal in this case:

(A) Whether claims 1-3 and 12-14 are obvious over Durec in view of Razavi; and

(B) Whether claims 4-11 and 15-18 are obvious over Bojer in view of Ravazi and Durec.

VII. ARGUMENT

A. Legal Standards

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810

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F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35.

It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine*, 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

B. Claims 1-3 and 12-14 are not obvious over Durec in view of Razavi.

Durec describes a frequency translation circuit 10 that translates an incoming reference signal to a lower frequency using a compound mixer circuit 42 that includes at least two mixers 14A-X. See Durec, Figures 1 and 4 and related discussion. The mixers 14A-X described in

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Durec each comprise four interconnected (stacked) transistors 66, 68, 70, 72. However, as admitted by the Examiner, Durec fails to teach or suggest a multiplier circuit having a first and a second mixer, the first mixer comprising a first number of transistors and the second mixer comprising a second number of transistors, the first number being different than the second number, as set forth in claims 1 and 4. The Examiner therefore relies upon Razavi to teach a mixer having two transistors.

The Examiner's conclusory statement that it would have been obvious to substitute one of the mixers described in Razavi for only one of the mixers described in Durec notwithstanding, Applicants respectfully submit that the cited references provide no suggestion or motivation to combine and modify the references in the manner suggested by the Examiner. To the contrary, Durec teaches away from a multiplier circuit having two mixers with an unequal number of transistors. For example, the four transistors in each of the mixers described in Durec are interconnected (stacked) in a manner that requires the presence of all four transistors in each mixer. Furthermore, the mixers described in Durec are interconnected with each other in a manner that requires that each mixer have the same number of transistors as the other mixers. Thus, Durec teaches away from combining the two-transistor mixer described by Razavi with the four-transistor mixers described by Durec to arrive at the invention set forth in independent claim 1 and claims 2-3 and 12-14 depending therefrom.

For at least the aforementioned reasons, Appellants respectfully submit that the Examiner has failed to make a *prima facie* case that claims 1-3 and 12-14 are obvious over Durec in view of Ravazi. Appellants request that the Examiner's rejections of claims 1-3 and 12-14 under 35 U.S.C. 103(a) be REVERSED.

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C. **Claims 4-11 and 15-18 are obvious over Bojer in view of Ravazi and Durec.**

Bojer describes a pair of multiplier circuits having four transistors each. The multiplier circuits receive four-phase signals from a generator. Bojer, however, fails to remedy the fundamental deficiency in the Durec and Razavi references, *i.e.* the failure to teach or suggest a first mixer comprising a first number of transistors and the second mixer comprising a second number of transistors, the first number being different than the second number, as set forth in claim 4. Accordingly, the cited references also fail to teach or suggest a second multiplier circuit having a third and a fourth mixer, the third mixer comprising a third number of transistors and the fourth mixer comprising a fourth number of transistors, the third number being different than the fourth number.

The cited references also fail to provide any suggestion or motivation to combine and/or modify the prior art of record to arrive at the invention claimed in claim 4. To the contrary, both Durec and Bojer teach away from the invention set forth in claim 4. As discussed above, Durec teaches away from a multiplier circuit having two mixers with an unequal number of transistors. Bojer also teaches away from a multiplier circuit having two mixers with an unequal number of transistors by teaching that the quadrature mixer 40 is a dual balanced quadrature mixer. See Bojer col. 3, ll. 64-65 and Figure 3. For example, the two balanced mixers (Gilbert cells 60, 62) each have four transistors T1-T8.

For at least the aforementioned reasons, Appellants respectfully submit that the Examiner has failed to make a *prima facie* case that claims 4-11 and 15-18 are obvious over Bojer in view of Durec and Ravazi. Appellants request that the Examiner's rejections of claims 4-11 and 15-18 under 35 U.S.C. 103(a) be REVERSED.

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VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1-18 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

There is no separate Evidence Appendix for this appeal.

X. RELATED PROCEEDINGS APPENDIX

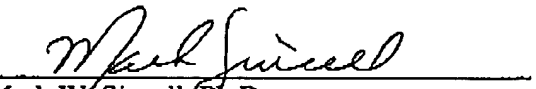
There is no Related Proceedings Appendix for this appeal.

XI. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-18, over the prior art of record. The undersigned may be contacted at (713) 934-4052 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

Date: 5/4/05



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CLAIMS APPENDIX

1. A mixer comprising:

a multiplier circuit having a first and a second mixer, the first mixer comprising a first number of transistors and the second mixer comprising a second number of transistors, the first number being different than the second number; and

a generator for generating two first and two second control signals for controlling said first and second mixers,

wherein said two first control signals have a frequency f_1 and said two second control signals have a different frequency f_2.

2. The mixer of claim 1, wherein said two first and two second control signals are balanced signals.

3. The mixer of claim 1, wherein said two first and two second control signals are single-ended signals.

4. A mixer for I/Q quadrature signal generation, comprising:

a first multiplier circuit having a first and a second mixer, the first mixer comprising a first number of transistors and the second mixer comprising a second number of transistors, the first number being different than the second number;

a second multiplier circuit having a third and a fourth mixer, the third mixer comprising a third number of transistors and the fourth mixer comprising a fourth number of transistors, the third number being different than the fourth number; and

a generator for generating two first and two second control signals for controlling said first and second mixers and two third and two fourth control signals for controlling said third and fourth mixers,

wherein said two first, two second, two third and two fourth control signals are in each case balanced signals, whereby said two first and two third control signals have a

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frequency f_1 and said two second and two fourth control signals have a different frequency f_2, and

either said signals at frequency f_1 or at frequency f_2 are provided in four phases each shifted by $\pi/2$.

5. The mixer of claim 4, wherein said first and second multiplier circuits each comprise a Gilbert cell having a plurality of transistors, where all transistors are used as switches.

6. The mixer of claim 4, wherein said generator comprises a frequency derivation circuit.

7. The mixer of claim 4, wherein the frequencies f_1 and f_2 of said control signals differ from an operation frequency of said generator.

8. The mixer of claim 6, wherein the frequency derivation within said frequency derivation circuit is executed by using frequency division.

9. The mixer of claim 6, wherein the frequency derivation within said frequency derivation circuit is executed by using frequency multiplication.

10. The mixer of claim 8, wherein voltages or currents within the circuit avoid the sum frequency $f_1 + f_2$.

11. The mixer of claim 8, wherein voltages or currents within the circuit avoid the difference frequency $f_1 - f_2$.

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12. The mixer of claim 1, wherein the first mixer comprises two transistors and the second mixer comprises four transistors.

13. The mixer of claim 1, wherein the two first control signals are complementary and the two second control signals are complementary.

14. The mixer of claim 1, wherein said multiplier circuit comprises a Gilbert cell having a plurality of transistors, where all transistors are used as switches.

15. The mixer of claim 4, wherein the first mixer comprises two transistors and the second mixer comprises four transistors.

16. The mixer of claim 4, wherein the third mixer comprises two transistors and the fourth mixer comprises four transistors.

17. The mixer of claim 4, wherein the two first control signals at frequency f_1 are complementary and the two third control signals at frequency f_1 are complementary.

18. The mixer of claim 4, wherein said control signals at frequency f_2 are provided in four phases each shifted by $\pi/2$.

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